

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appellants:	Cogdill et al.	Patent Application	
Application Number:	10/655,964	Group Art Unit:	2819
Filed:	September 4, 2003	Examiner:	Tran, J.
For:	CIRCUIT AND SYSTEM FOR ADDRESSING MEMORY MODULES		

REPLY BRIEF

In response to the Examiner's Answer mailed on December 16, 2009, Appellants respectfully submit the following remarks.

REMARKS

Appellants are submitting the following remarks in response to the Examiner's Answer. In these remarks, Appellants are addressing certain arguments presented in the Examiner's Answer. While only certain arguments are addressed in this Reply Brief, this should not be construed that Appellants agree with the other arguments presented in the Examiner's Answer.

Response to Argument on Page 10, Last Paragraph, through Page 11, Second Paragraph of the Examiner's Answer

In the Appeal Brief filed June 2, 2009, while addressing a 35 U.S.C. §102(e) of Claims 1-5, 7-19 and 21 and a 35 U.S.C. §103(a) rejection of Claims 6, 20 and 22, and in particular independent Claim 1, Appellants argue that Johnson et al. (U.S. Patent No. 6,715,014)(hereinafter, "Johnson") does not anticipate or suggest:

A circuit for a memory module address bus comprising:
a transmission line comprising a series dampening impedance between a driver and a branch point of said transmission line; and
a parallel termination impedance having one end coupled to said transmission line between said series dampening impedance and said branch point, wherein said parallel termination impedance is on a same side of all memory modules as said driver;
said transmission line having branches from said branch point, wherein ones of said branches are coupled to at least one memory module interface.

as is recited in Appellants' Claim 1.

Appellants further pointed out that the particular structure (positioning of its parallel termination impedance) as recited in Claim 1 has a distinct advantage over the structure as is described in Johnson's Figure 3:

Referring briefly to Figure 1, the purpose of the pull-up parallel termination resistor 130 is to terminate the signal at the end of the transmission line 115. As such, it is not considered intuitive to place a parallel termination resistor on the same side of the memory modules as the driver. Referring now to Figure 2, the termination impedance 360 is placed on the same side of the memory modules 340 as the driver 305. As positioned, the combination of the series dampening impedance 350 and the parallel termination impedance 360 prevents, or at least reduces, reflections from the memory modules 340 from travelling back to the driver 305 in the region of the transmission line 320a between the parallel termination resistor 360 and the driver 305. There may be some reflections in the region of the transmission line 320b between the parallel termination resistor 360 and the branch point 315, as well as on the branches of the transmission line 320c and 320d.

However, embodiments of the present invention are configured such that reflections between the parallel termination resistor 360 and the memory modules 340 do not cause significant signal integrity problems. For example, the memory modules 340 are located very close to each other relative to the size of the wavelength of a typical signal.

(Appellants' specification, second and third paragraph.)

The Examiner's Answer states:

The Examiner would like to note that the circuit as shown below (Figure 3b) is **equivalent** to the circuit shown in Figure 3 of Johnson. The Examiner would also like to add that it is irrelevant how these schematics are drawn as long as the connections/nodes are the same, since it is merely a matter of drawing choice.

(Examiner's Answer, page 10, last paragraph.) The Examiner's Answer then shows a drawing of a "Figure 3(b)" that is neither the Figure 3B that is part of Appellants' specification, nor the Figure 3 that is part of Johnson's disclosure. Additionally, the "lead-in transmission line 314" is missing from the Figure 3(b) shown in the Examiner's Answer.

Moreover, as shown in Johnson's Figure 3, Johnson states an advantage of the particular star like pattern positioning around the branch point of the "terminating impedance 326" and the "series impedance 324" is as follows:

From the foregoing it will be appreciated that the star-stub topology provided by the invention helps improve the signal characteristics of signals received by industry standard open stub memory modules or other types of modules. The topology is easier to realize than a pure star topology and provides better signal characteristics than a pure comb topology.

(Johnson, column 3, lines 1-7.)

Thus, Appellants respectfully submit that the schematics of Johnson's Figure 3 is relevant to the Johnson's disclosure within its specification. An alteration of Johnson's schematics to be that of Figure 3(b) of the Examiner's Answer would alter and defeat the objective of the "star-stub topology" of Johnson's Figure 3, as explained herein.

CONCLUSION

In view of the above remarks, Appellants continue to assert that Johnson does not anticipate Appellants' Claims 1-5, 7-19 and 21 for reasons presented above and for reasons previously presented in the Appeal Brief. Furthermore, Appellants continue to assert that Claims 6 and 20 are patentable over Johnson in view of Buuck et al. (U.S. Patent Application No. 5,583,449) for reasons presented above and for reasons previously presented in the Appeal Brief. Moreover, Appellants continue to assert that Claim 22 is patentable over Johnson in view of Mizukami et al. (U.S. Patent Application No. 5,111,080) for reasons presented above and for reasons previously presented in the Appeal Brief.

Respectfully submitted,
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Dated: 02/12/2010

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